

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

- 1 1. (currently amended) A computer-readable storage medium having a
2 stored computer-executable instruction set for initiating a method of driving
3 the simulation testing of a design of an integrated circuit (IC) which is to be
4 incorporated into an intended system comprising the steps of:
5 providing an asynchronous sequence of states configured for
6 simulating operating conditions relevant to driving sequencing of signal-
7 exchange events with said IC;
8 identifying first upper and first lower parameters of timing
9 constraints imposed by said intended system with respect to enabling
10 individual said events;
11 forming a first synchronous sequence of states in which said
12 states are synchronized on a basis of remaining within said first upper and
13 first lower parameters of timing constraints;
14 identifying second upper and second lower parameters of timing
15 constraints imposed by said IC with respect to enabling individual said events;
16 forming a second synchronous sequence of states in which said
17 states are synchronized on a basis of remaining within said second upper and
18 said second lower parameters of timing constraints; and
19 using said second synchronous sequence as a basis for said
20 simulation testing of said design.
- 1 2. (currently amended) A computer-readable storage medium having
2 computer-executable program code configured to implement a method of
3 generating a synchronous sequence of test vectors from information
4 originating within an asynchronous environment comprising:
5 providing a simulation synchronous sequence of states,
6 wherein each of said states is referenced to a clock period, said simulation
7 synchronous sequence being partially based on event timing parameters of
8 a particular system of interest;

9 introducing short timing delays to said states within specific said
10 clock periods of said simulation synchronous sequence to generate an
11 asynchronous short-delay sequence of states, durations of specific said short
12 timing delays being responsive to event timing parameters of a particular
13 integrated circuit (IC) design;
14 comparing said states of said asynchronous short-delay
15 sequence, including correlating a plurality of said clock periods having said
16 states of said asynchronous short-delay sequence to identify a first over-
17 lapping time interval, said first overlapping time interval being consistent with
18 a time coincidence among said states of said asynchronous short-delay
19 sequence;
20 generating a synchronous short-delay sequence by successively
21 repeating a first delay-adjusted clock period having a state which is delayed
22 by said first overlapping time interval;
23 introducing long timing delays to said states within specific
24 said clock periods of said simulation synchronous sequence to generate
25 an asynchronous long-delay sequence of states, durations of specific said
26 long timing delays being responsive to event timing parameters of said
27 particular IC design;
28 comparing said states of said asynchronous long-delay
29 sequence, including correlating a plurality of said clock periods having said
30 states of said asynchronous long-delay sequence to identify a second
31 overlapping time interval, said second overlapping time interval being
32 consistent with a time coincidence among said states of said asynchronous
33 long-delay sequence;
34 generating a synchronous long-delay sequence by successively
35 repeating a second delay-adjusted clock period having a state which is
36 delayed by said second overlapping time interval; and
37 comparing said synchronous short-delay sequence with timing
38 of said states of said synchronous long-delay sequence to generate said
39 synchronous sequence of test vectors, including time aligning said
40 synchronous short-delay and long-delay sequences to detect a plurality of
41 overlapping sampling time intervals for locating said synchronous sequence of
42 test vectors.

1 3. (currently amended) The storage medium ~~method~~ of claim 2 wherein said
2 step of introducing said short timing delays includes adding best case tester-
3 load timing delays to said clock periods of said simulation synchronous
4 sequence, said best case tester-load timing delays being indicative timing
5 constraints of an IC tester.

1 4. (currently amended) The storage medium ~~method~~ of claim 2 wherein said
2 step of introducing said short timing delays includes adding best case chip-
3 load timing delays indicative of timing constraints of said IC design.

1 5. (currently amended) The storage medium ~~method~~ of claim 3 wherein said
2 step of introducing said long timing delays includes adding worst case tester-
3 load timing delays that are indicative of said timing constraints of said IC
4 tester.

1 6. (currently amended) The storage medium ~~method~~ of claim 4 wherein said
2 step of introducing said long timing delays includes adding worst case chip-
3 load timing delays indicative of said timing constraints of said IC design.

1 7. (currently amended) The storage medium ~~method~~ of claim 2 wherein said
2 step of providing said simulation synchronous sequence includes:
3 providing a simulated asynchronous sequence of states;
4 extracting a state of said asynchronous sequence at each said
5 clock period to generate a simulated synchronous sequence of states;
6 introducing an abbreviated timing delay to each said clock
7 period of said simulated synchronous sequence to generate a simulated
8 synchronous abbreviated-delay sequence and introducing an extended timing
9 delay to each said clock period of said simulated synchronous sequence to
10 generate a simulated synchronous extended-delay sequence; and
11 comparing said simulated synchronous abbreviated-delay
12 sequence to said simulated synchronous extended-delay sequence, including
13 time aligning said simulated synchronous abbreviated-delay and extended-
14 delay sequences to detect a plurality of overlapping second time intervals
15 for defining positions of states in said clock periods of said simulation
16 synchronous sequence.

1 8. (currently amended) The storage medium ~~method~~ of claim 7 wherein said
2 step of introducing said abbreviated timing delay and said extended timing
3 delay includes executing said simulated synchronous sequence under
4 respective best case timing delay and worst case timing delay scenarios in a
5 system simulation environment, said system simulation environment having
6 timing characteristics indicative of said particular system of interest.

1 9. (currently amended) The storage medium ~~method~~ of claim 7 further
2 including adapting said simulated synchronous extended-delay sequence as
3 said simulation synchronous sequence when there is not an acceptable
4 number of said overlapping second time intervals.

1 10. (currently amended) The storage medium ~~method~~ of claim 7 wherein
2 said step of providing said simulated asynchronous sequence includes
3 selecting said clock period to have a duration that corresponds to a tester
4 clock period of an IC tester.

1 11. (currently amended) The storage medium ~~method~~ of claim 2 further
2 including selectively fixing a sampling instance in one of said overlapping
3 sampling time intervals to correspond to a rising edge of a tester clock period
4 of an IC tester.

1 12. (currently amended) A computer-readable medium having executable
2 instructions for driving a test vector generator for generating a synchronous
3 sequence of test vectors, such that said executable instruction and test vector
4 generator are cooperative to comprise: comprising:
5 a simulation module that is enabled to generate a simulation
6 synchronous sequence of states under a system simulation environment, said
7 simulation synchronous sequence including a plurality of timing regions for
8 identifying operations of an integrated circuit (IC) design;
9 a delay module that is enabled to introduce short delays and
10 long delays to said simulation synchronous sequence to respectively generate
11 asynchronous short-delay sequence and asynchronous long-delay sequence,
12 each of said short delays and said long delays being timing delays associated
13 with at least one of an integrated circuit (IC) and an IC tester;
14 an overlaying module that is configured to provide a first state
15 overlapping time interval and a second state overlapping time interval by
16 respectively comparing a plurality of base periods of said asynchronous
17 short-delay sequence and comparing a plurality of base periods of said
18 asynchronous long-delay sequence;
19 a duplication module that is configured to incorporate said first
20 state overlapping time interval into a first sequence of said base periods and
21 to incorporate said second state overlapping time interval into a second
22 sequence of said base periods to respectively generate a synchronous short-
23 delay sequence and a synchronous long-delay sequence; and
24 a sequence overlaying module that is configured to time align
25 said synchronous short-delay sequence and said synchronous long-delay
26 sequence to detect a plurality of overlapping sampling intervals for locating
27 said synchronous sequence of test vectors.

1 13. (currently amended) The computer-readable medium test-vector
2 generator of claim 12 wherein said executable instructions are configured
3 such that said short delays are related to a best case chip-load timing delay of
4 said IC and a best case tester-load timing delay of said IC tester.

1 14. (currently amended) The computer-readable medium test-vector
2 generator of claim 13 wherein said executable instructions are configured
3 such that said long delays are related to a worst case chip-load timing delay
4 of said IC and a worst case tester-load timing delay of said IC tester.

1 15. (currently amended) The computer-readable medium test-vector
2 generator of claim 12 wherein said executable instructions are further
3 cooperative with said test vector generator to define further comprising a
4 verification module that is configured to execute said synchronous sequence
5 of test vectors under said short delays and said long delays for verifying
6 timing correctness.

1 16. (currently amended) The computer-readable medium test-vector
2 generator of claim 12 wherein said executable instructions are configured
3 such that said system simulation environment is independent of any delay
4 associated with said IC and said IC tester.

1 17. (currently amended) The computer-readable medium test-vector
2 generator of claim 12 wherein said executable instructions are configured
3 such that said base period is a time interval that is equivalent to a tester
4 period of said IC tester.

1 18. (currently amended) A program storage device having
2 computer-executable code for implementing a method for converting
3 asynchronous states into synchronous states to generate a synchronous
4 sequence of test vectors for verifying functionality of a simulated integrated
5 circuit (IC) design comprising:
6 providing a simulation synchronous sequence of states;
7 generating an asynchronous short-delay sequence of first
8 periods and an asynchronous long-delay sequence of second periods,
9 including inserting short delays and long delays into said simulation
10 synchronous sequence, said short delays and said long delays characterizing
11 timing delays of at least one of said simulated IC and a tester;
12 detecting a short-delay overlapping time interval and a long-
13 delay overlapping time interval, including correlating a plurality of said first
14 periods to identify said short-delay overlapping time interval and correlating a
15 plurality of said second periods to identify said long-delay overlapping time
16 interval;
17 generating a synchronous short-delay sequence of states by
18 forming a succession of substantially identical base periods that include a
19 state and said short-delay overlapping time interval;
20 generating a synchronous long-delay sequence of states by
21 forming a succession of substantially identical base periods that include a
22 state and said long-delay overlapping time interval; and
23 generating said synchronous sequence of test vectors, including
24 time-aligning said synchronous short-delay sequence and said synchronous
25 long-delay sequence and identifying overlapping timing envelopes of states
26 within corresponding said base periods of said synchronous short-delay and
27 long-delay sequences.

1 19. (currently amended) The program storage device method of claim 18
2 wherein said step of inserting said short delays and said long delays includes
3 respectively introducing best-case timing delays of said IC and worst-case
4 timing delays of said simulated IC.

1 20. (currently amended) The program storage device method of claim 19
2 wherein said step of inserting said short delays and said long delays includes
3 respectively introducing best-case timing delays of said tester and worst-case
4 timing delays of said tester.